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Research on Improvement of LED Lamp Production Line Based on FlexSim

Junyang Tian *, Ziheng Zhang

Southwest Petroleum University, Chengdu, China

Abstract: Addressing the core issues of low production line balance rate, severe idle human resources, and limited production capacity in a certain LED lamp assembly line, this study comprehensively employs the stopwatch time study method, the Westinghouse Rating System, and production line balancing theory to systematically diagnose the current state of the production line. Through work measurement, it identifies that the OP8 lamp board soldering station and the OP18 packaging station constitute a bimodal bottleneck. The original line's bottleneck cycle time reaches 43.089 seconds, the balance rate is only 49.65%, and the smoothness index is as high as 23.81, indicating severe "cycle time cliffs" and resource waste. Based on this, this paper proposes two differentiated improvement strategies: the efficiency-driven scheme (Scheme I) applies the ECRS principle to merge 18 workstations into 12. With no additional investment, it increases the balance rate to 74.48%, increases per capita output by over 50%, and achieves staff reduction and efficiency improvement. The capacity-expansion scheme (Scheme II), based on the Theory of Constraints, implements parallelization transformation for the bottleneck processes, compressing the cycle time to 21.545 seconds, raising the balance rate to 77.72%, reducing the smoothness index to 5.25, and doubling the theoretical single-shift capacity to 1,336 units. Finally, the FlexSim simulation software is used to dynamically verify the improvement schemes. The error between the simulated output and the theoretical calculation is controlled within 1%, confirming the effectiveness of the model and the robustness of the optimization schemes. This study indicates that enterprises can flexibly choose improvement paths based on their strategic phases of cost priority or scale priority, providing a reliable decision-making basis for lean production management.

Keywords: LED lamp assembly line, Work measurement, Line of Balance (LOB), ECRS principle, FlexSim simulation.

1. Introduction

1.1. Research Background and Significance

With the continuous advancement of global energy structure transformation and green and low-carbon development strategies, the LED lighting industry has ushered in broad market space. However, against the backdrop of increasingly fierce industry competition, LED lighting manufacturing enterprises not only need to cope with the shortening of product life cycles but also face the dual squeeze of raw material costs and labor costs. Traditional labor-intensive assembly models are gradually becoming key bottlenecks restricting corporate profit growth. How to systematically improve production line efficiency and reduce resource waste while ensuring product quality has become an urgent need for manufacturing enterprises in their transformation and upgrading.

Furthermore, with the popularization of Industry 4.0 and Digital Twin concepts, Discrete Event Simulation (DES) technology provides new technical pathways for the dynamic evaluation and quantitative optimization of complex manufacturing systems. Using computer simulation software (such as FlexSim) allows for low-cost, high-precision "sandbox simulations" of various improvement schemes without interrupting actual production, thereby providing support for scientific decision-making.

Based on the above practical dilemmas, this study holds significant theoretical and practical dual significance:

Theoretical significance: This study organically combines traditional industrial engineering theories (such as stopwatch time study, ECRS principles, and production line balancing theory) with advanced discrete event simulation technology, constructing a closed-loop optimization framework of "current diagnosis - theoretical deduction - simulation verification." By comparing the simulation effects of two differentiated strategies, "efficiency-driven" and "capacity-expansion", it deeply explores the logic of production line restructuring under different business orientations, enriches the theoretical application of lean production management in the LED assembly industry, and provides theoretical support for the implementation of Digital Twins in discrete manufacturing.

Practical significance: Based on the actual production line pain points of Company A, this study provides directly implementable engineering improvement schemes. Scheme I (ECRS merging and reorganization) can help enterprises achieve "staff reduction and efficiency improvement" during stable market periods without any additional fixed asset investment, effectively reducing labor costs. Scheme II (bottleneck parallelization transformation), on the other hand, can achieve a significant increase in output capacity through space-for-time trade-offs during peak order periods. The research ideas and data can not only directly guide Company A's lean transformation of its production line but also provide practical references for the digital transformation and production line upgrades of similar small and medium-sized lighting manufacturing enterprises.

1.2. Domestic and International Research Status

In the evolution path of solution algorithms, international research has successively gone through three stages: exact algorithms, heuristic algorithms, and intelligent optimization algorithms. Early stages mainly relied on exact algorithms such as linear programming and dynamic programming;

however, limited by the NP-hard nature of the Assembly Line Balancing Problem (ALBP), they could only solve small-scale problems. After the 1990s, meta-heuristic algorithms such as genetic algorithms, ant colony algorithms, and particle swarm algorithms gradually became the mainstream solution methods, significantly improving the efficiency and quality of solutions for medium and large-scale problems [1]. International research on ECRS rarely stays at the application of a single method but focuses more on its integration with other lean tools and simulation technologies. Chawana et al. (2024) combined the ECRS principle with the positional weight method and FlexSim simulation, applying them to a balancing improvement project for a car seat cover production line. By canceling redundant handling processes, merging auxiliary operations, rearranging process sequences, and simplifying operational actions, they ultimately improved both the production line balance efficiency and daily output, forming a standardized research paradigm of "qualitative process improvement + quantitative simulation verification" [2]. Sae-Lim and Thongmak (2023) applied the four ECRS principles to the balance optimization of a gas stove parts stamping production line. By canceling non-value-added inspection processes, merging adjacent stamping operations, and rearranging the processing flow, they reduced the number of workstations by 2 and increased the production line capacity by 28%, validating the improvement value of the ECRS method in discrete processing scenarios [3]. Kotrady et al. (2026) built an assembly line simulation model considering operator skill differences based on FlexSim, verifying the dual improvement effect of intelligent operator rotation mechanisms on workstation load balance and overall equipment utilization, thus expanding the application boundaries of FlexSim in the dynamic optimization of production systems [4].

Domestic research on production line balancing started in the 1990s. Initially focused on introducing and digesting foreign theoretical methods, it gradually formed a localized research characteristic of "theoretical method improvement + industry application validation." Sun Jianhua et al. (2004) systematically summarized the technical means and methodological systems for production line balancing at an early stage, proposing a combined application path of industrial engineering methods and mathematical programming methods, providing early methodological guidance for the line balancing practices of domestic manufacturing enterprises [5]. Zhu Huabing et al. (2013) were among the early adopters who combined the ECRS principle with process reorganization methods and applied them to the production line balance improvement of a motor assembly line. Their study effectively improved the balance rate and production efficiency by canceling redundant inspection processes, merging adjacent assembly operations, rearranging process sequences, and simplifying fastener installation actions. This work became a classic literature in the domestic application of ECRS and has been widely cited by subsequent research [6]. FlexSim was introduced to China around 2005. With the advancement of digital transformation in domestic manufacturing, its application research has grown rapidly and has now become one of the most commonly used simulation software in the field of industrial engineering in China. In the domain of production line balance optimization, the domestic academic community has formed a mature research path of "FlexSim modeling and simulation + industrial engineering improvement methods." Liu Wen et al. (2025) built a digital simulation model on the FlexSim platform for a customized door and window machining production line. By customizing programs to improve the simulation logic, they accurately identified the drilling and milling hole-making process as the system bottleneck and proposed optimization schemes combined with the ECRS principle, validating the applicability of simulation methods in customized production scenarios [7]. In addition to manufacturing production lines, FlexSim is also widely used in logistics, mining, and other industries. Wu Donglong et al. (2020) applied FlexSim to the simulation and optimization of a coal main production logistics system. Through modeling and analysis, they identified the main shaft hoisting equipment as the core bottleneck of the system. After equipment configuration optimization, the overall system operational efficiency was significantly improved [8]. Chu Yanfeng et al. (2023) addressed the parallel production system of grouped products by incorporating process complexity and employee skill differences into a balance optimization model. They designed a corresponding solution algorithm to achieve precise matching between process load and personnel capability, expanding the constraint dimensions and engineering applicability of the line balancing problem [9]. Chen Jiaxin et al. (2024) conducted a balance optimization study on a women's trousers production line based on an improved ECRS method. Through process rearrangement and work content adjustment, they increased the line's compilation efficiency from 65.83% to 90.89% and daily output by 38.30%, demonstrating a very significant improvement effect [10].

1.3. Research Content and Technical Route

This study first employs the stopwatch time study method and the Westinghouse Rating System to determine standard times. It uses the 3σ rule to eliminate outliers. By calculating the production line balance rate and smoothness index, it systematically diagnoses the "bimodal" bottlenecks and severe cycle time cliff issues present in the original line. To address the current situation, two differentiated restructuring schemes are designed: Scheme I utilizes the ECRS principle to merge and reduce the 18 workstations, aiming to achieve staff reduction and efficiency improvement without additional investment. Scheme II, based on the Theory of Constraints, implements parallelization transformation for the bottleneck processes to break through the capacity ceiling. Finally, the FlexSim simulation software is used to construct models for the current state and the improved schemes for verification. The advantages and disadvantages of each scheme in terms of balance rate, capacity, and per capita output are comprehensively compared, thereby providing a scientific basis for decision-making regarding lean production line transformation for enterprises under different strategic orientations of "cost priority" or "scale priority."

2. Current Status Investigation and Problem Identification of the Assembly Line

2.1. Production Process Overview

Company A is a lamp manufacturing company, primarily engaged in the production of various types of LED lamps. Its main product is a 3W LED lamp. The production process involves: solder paste printing, component placement, reflow soldering, lamp board testing, applying thermal conductive

silicone grease to the lamp board, inserting the constant current board into the PC tube, threading the power cord through the heat sink, soldering wires to the lamp board, securing the lamp board with screws to the heat sink, applying silicone glue to fix the constant current board, installing the lamp holder, FQC inspection, installing the translucent cover, dotting the lamp holder, visual inspection and cleaning, functional testing, and packaging.

2.2. Work Measurement and Calculation of Standard Time (Tstd)

2.2.1. Observation Objects and Timing Tools

To obtain true and accurate operational data, this study used the "stopwatch time study method" to conduct on-site measurements of each process on the LED lamp assembly line. The observation objects were the 18 workstations (OP1-OP18) and their corresponding operators on the assembly line. To ensure data representativeness, observations were conducted during regular shifts when the production line was operating smoothly. The observed employees had all undergone professional training, with their proficiency levels being average. No targeted speed-up was conducted during the observation period, ensuring that the measured data genuinely reflected the existing work intensity and process level. This study employed the continuous timing method, performing complete work cycle measurements for each process, strictly timing according to the "start point" and "end point" of each operation. Considering the high repetitiveness and relatively stable cycle times of assembly operations, the initial sample size was set at n=10. The measurement data are shown in Table 1:

Table 1. Record of the first 10 observation times for the LED lamp assembly line

Process No.	Process Name	1st (s)	2nd (s)	3rd (s)	4th (s)	5th (s)	6th (s)	7th (s)	8th (s)	9th (s)	10th (s)
OP1	Solder Paste Printing	9.1	8.8	9.2	9.6	8.8	8.8	9.6	9.2	8.7	9.1
OP2	Component Placement	13.1	13.1	13.6	12.1	12.2	13	12.7	13.6	12.8	12.5
OP3	Reflow Soldering	19.4	17.9	18.2	16.8	17.6	18.2	17.1	18.4	17.6	17.8
OP4	Lamp Board Testing	13.1	14.8	13.5	12.8	14.1	12.7	13.6	12.2	12.6	13.6
OP5	Apply Thermal Grease	13.8	13.4	13.2	13.1	12.3	12.8	13	14	13.5	12.1
OP6	Insert Board into PC Tube	12.4	12	11.8	12.6	12.8	12.8	11.7	12	12.4	12.8
OP7	Thread Wire through Heat Sink	15.7	16	15.2	15.1	16.8	17.2	16	16.9	16.4	15.6
OP8	Lamp Board Wire Soldering	36.5	38.7	35.8	38.7	31.2	37.4	36.1	35.4	36.1	32.3
OP9	Screw Board to Heat Sink	13.8	14.2	15	13.6	13.4	13.6	14.6	14.2	13.6	14.4
OP10	Apply Silicone to Board	13.9	14.5	13.3	13.6	13.5	12.8	14	14	13.8	13.6
OP11	Install Lamp Holder	25.1	26.4	26.5	25.9	26.8	27.5	29.5	27.2	27.3	26.9
OP12	FQC Inspection	13.6	15	15	15.8	14.9	15.2	15	14.1	15.9	15.6
OP13	Install Translucent Cover	27.7	25.4	28.5	24.7	27.4	29.5	25.3	25.8	26.7	25.9
OP14	Light Emission Test	8.3	9	8.5	9.2	8.6	9.7	8.6	8.9	9.4	8.4
OP15	Dot Lamp Holder	13.7	14.4	12.4	13.6	13.7	14	12.7	12.6	13.9	13.7
OP16	Visual Inspection & Cleaning	27.4	27.6	26.2	27.4	27.5	26.1	29.6	27.7	25.5	28
OP17	Functional Testing	13.3	14.6	14.8	13.4	14.7	14.3	14.6	15.3	13.8	13.5
OP18	Packaging	34.4	34.5	35.9	36.6	36.5	37.5	36	38.6	35.5	40.9

2.2.2. Observation Data Processing

Since on-site observations may be affected by random factors such as environmental interference, fluctuations in part quality, or momentary operator fatigue, the measured data may contain "outliers" that deviate from the normal level. To ensure the accuracy of subsequent modeling parameters, this study adopted the "three-sigma rule (3σ rule)" to screen and eliminate outliers from the 10 original measurements for each process.

For the observation sequence of each process x1, x2, …, xn(where n=10), the arithmetic mean x and sample standard deviation s are first calculated:

$$\bar{x} = \frac{1}{n}\sum_{i=1}^{n} x_i$$

When calculating the sample standard deviation s, due to the small observation sample size (n=10), to correct for the estimation bias of the population variance by the sample mean, this study uses the sample standard deviation after Bessel's correction, ensuring the scientific rigor and robustness of the outlier elimination criterion.

$$s = \sqrt{\frac{\sum_{i=1}^{n}(x_i - \bar{x})^2}{n-1}}$$

According to statistical normal distribution theory, the valid interval for observations is set to $[\bar{x} - 3s, \bar{x} + 3s]$. If an observation xi satisfies $|x_i - \bar{x}| > 3s$, it is determined to be an outlier and must be eliminated, and the mean of the remaining data must be recalculated. The calculation process and results are shown in Table 2:

Table 2. Summary of data cleaning using the three-sigma rule

Process No.	Process Name	Mean ($\bar{x}$)	Std Dev (s)	LCL ($\bar{x}-3s$)	UCL ($\bar{x}+3s$)	Outliers	Cleaned Mean
OP1	Solder Paste Printing	9.09	0.325	8.115	10.065	None	9.09
OP2	Component Placement	12.87	0.517	11.319	14.421	None	12.87
OP3	Reflow Soldering	17.9	0.724	15.728	20.072	None	17.9
OP4	Lamp Board Testing	13.3	0.779	10.963	15.637	None	13.3
OP5	Apply Thermal Grease	13.12	0.605	11.305	14.935	None	13.12
OP6	Insert Board into PC Tube	12.33	0.427	11.049	13.611	None	12.33
OP7	Thread Wire through Heat Sink	16.09	0.72	13.93	18.25	None	16.09
OP8	Lamp Board Wire Soldering	35.82	2.441	28.497	43.143	None	35.82
OP9	Screw Board to Heat Sink	14.04	0.523	12.471	15.609	None	14.04
OP10	Apply Silicone to Board	13.7	0.459	12.323	15.077	None	13.7
OP11	Install Lamp Holder	26.91	1.156	23.442	30.378	None	26.91
OP12	FQC Inspection	15.11	0.889	12.443	17.777	None	15.11
OP13	Install Translucent Cover	26.69	1.552	22.034	31.346	None	26.69
OP14	Light Emission Test	8.86	0.462	7.474	10.246	None	8.86
OP15	Dot Lamp Holder	13.47	0.667	11.469	15.471	None	13.47
OP16	Visual Inspection & Cleaning	27.3	1.154	23.838	30.762	None	27.3
OP17	Functional Testing	14.23	0.686	12.172	16.288	None	14.23
OP18	Packaging	36.64	1.961	30.757	42.523	None	36.64

2.2.3. Determination of Rating Factor and Allowance Rate

This study uses the Westinghouse Rating System to qualitatively evaluate the operators' performance. This method evaluates comprehensively across four dimensions: Skill, Effort, Conditions, and Consistency. Based on on-site observations and combined with evaluations from the workshop production supervisors, the comprehensive rating values for the operators on this LED lamp assembly line are shown in Table 3:

Table 3. Comprehensive rating value table

Evaluation Dimension	Grade	Score	Description
Skill	C1 (Good)	0.06	Smooth movements, high precision in component alignment.
Effort	D (Average)	0	Positive work attitude, able to maintain a steady work pace.
Conditions	D (Average)	0	Ambient temperature, lighting, and noise meet national standards.
Consistency	E (Fair)	-0.01	Slight fluctuations in cycle times due to manual operations.
Comprehensive Result		0.05	Rating Factor R=1+0.05=1.05

Since operators will inevitably be affected by physiological needs, psychological fatigue, and random production interruptions during actual work, allowance time must be added to the normal time. Referring to international standard allowance rates, and considering the actual labor intensity of the LED lamp workshop (medium physical labor), this paper sets the comprehensive allowance rate at 12%, composed of the following:

Physiological allowance (3%): To meet basic physiological needs such as drinking water and restroom breaks.

Fatigue allowance (5%): To compensate for physical and mental fatigue caused by prolonged repetitive assembly operations.

Procedural allowance (4%): To handle random interferences during the operation, such as tool adjustments and necessary inter-process communication.

Therefore, the comprehensive allowance factor is A=3%+5%+4%=12%.

2.2.4. Standard Time Calculation

Based on the previously determined rating factor R=1.05 and the comprehensive allowance rate A=12%, the standard time for each process on the LED lamp assembly line is calculated using the formula. The formula for Standard Time (T_{std}) is:

$$T_{std} = \bar{T} \times R \times (1 + A)$$

Where $\bar{T}$ is the average observed time after data cleaning.

Taking process OP1 (Solder Paste Printing) as an example, its average observed time after 3σ cleaning is $\bar{T}_1$=9.09s, Substituting into the model:

$$T_{std,1} = 9.09 \times 1.05 \times (1 + 12\%) = 10.69s$$

The complete calculation process is shown in Table 4:

Table 4. Standard time calculation table

Process No.	Process Name	Cleaned Mean $\bar{T}$(s)	Normal Time Tnorm (s)	Standard Time Tstd (s)
OP1	Solder Paste Printing	9.09	9.545	10.69
OP2	Component Placement	12.87	13.514	15.136
OP3	Reflow Soldering	17.9	18.795	21.05
OP4	Lamp Board Testing	13.3	13.965	15.641
OP5	Apply Thermal Grease	13.12	13.776	15.429
OP6	Insert Board into PC Tube	12.33	12.946	14.5
OP7	Thread Wire through Heat Sink	16.09	16.894	18.921
OP8	Lamp Board Wire Soldering	35.82	37.611	42.124
OP9	Screw Board to Heat Sink	14.04	14.742	16.511
OP10	Apply Silicone to Board	13.7	14.385	16.111
OP11	Install Lamp Holder	26.91	28.256	31.647
OP12	FQC Inspection	15.11	15.866	17.77
OP13	Install Translucent Cover	26.69	28.025	31.388
OP14	Light Emission Test	8.86	9.303	10.419
OP15	Dot Lamp Holder	13.47	14.144	15.841
OP16	Visual Inspection & Cleaning	27.3	28.665	32.105
OP17	Functional Testing	14.23	14.942	16.735
OP18	Packaging	36.64	38.472	43.089

2.3. Quantitative Evaluation of the Current State

After determining the standard times for all processes, this study selects the Line of Balance (LOB), Smoothness Index (SI), and theoretical capacity (P) as quantitative evaluation indicators to systematically assess the operational efficiency of the LED assembly line.

2.3.1. Definition of Evaluation Indicators and Formulas

(1) Line of Balance (LOB): Reflects the degree of load balance among workstations.

$$\mathrm{LOB} = \frac{\sum_{i=1}^{n} T_{std,i}}{S \times CT} \times 100\%$$

Where S is the number of workstations (S=18), and CT is the bottleneck cycle time($\max\{T_{std,i}\}$).

(2) Smoothness Index (SI): Measures the fluctuation amplitude of workstation times relative to the bottleneck time.

$$\mathrm{SI} = \sqrt{\frac{\sum_{i=1}^{n}(CT - T_{std,i})^2}{n}}$$

The closer the SI value is to 0, the more consistent the load across the workstations.

(3) Theoretical Capacity (P): The total output in an ideal state per unit time.

$$P = \frac{T_{total}}{CT}$$

Where T_{total} is the effective working time per shift (taking $8 \times 3600 = 28800s$).

Calculated using the above methods, the results are: Line of Balance LOB≈49.65%, Smoothness Index SI≈23.81, Theoretical Capacity P≈668 units/shift. This set of data indicates that the current LED lamp assembly line suffers from severe efficiency bottlenecks and resource redundancy. The extremely low balance rate of 49.65% indicates that over half of the workforce's time is spent in non-value-added waiting states, resulting in low conversion efficiency of labor costs. The high smoothness index of 23.81 quantifies the severe fluctuations in workload between processes, revealing serious disruptions in production rhythm and hidden dangers of massive Work-In-Progress (WIP) accumulation. Furthermore, the theoretical capacity of merely 668 units per shift renders the system completely lacking the flexibility to respond to high demand fluctuations. In summary, the production line has significant optimization potential in terms of process arrangement and resource allocation.

2.4. Bottleneck and Waste Analysis

After completing the quantitative evaluation of the current state, to deeply analyze the root causes behind the low balance rate and high volatility, this section will systematically identify and qualitatively analyze the bottlenecks and wastes existing in the production line from three dimensions: cycle time span, human resource allocation, and process fluctuation. This provides direction for the subsequent optimization scheme design based on the ECRS principle.

2.4.1. Bottleneck Identification Based on Cycle Time Span

Based on the standard times (Tstd) of each process, a significant "long-tail effect" and "cycle time cliff" can be observed intuitively. The current bottleneck cycle time (CT) is the 43.09s of OP18 (Packaging), followed by the 42.12s of OP8 (Lamp Board Wire Soldering).

From the perspective of cycle time span distribution, the overall process times show severe polarization:

Very High Cycle Time Zone (>30s): Includes OP8 (42.12s), OP11 (31.65s), OP13 (31.39s), OP16 (32.11s), and OP18 (43.09s). The sum of the times for these 5 processes accounts for 46.7% of the total standard time of the entire process flow, yet they represent only 27.8% of the process count. Notably, OP8 and OP18 have times that are 1.97 times and 2.01 times the overall process mean (21.4s), respectively, forming a "bimodal" bottleneck that severely drags down the overall output rhythm.

Very Low Cycle Time Zone (<15s): Includes OP1 (10.69s), OP6 (14.5s), OP14 (10.42s), etc. Workers at these stations require only about 10-14 seconds per cycle but are forced to wait for over 30 seconds of idle time due to blockages caused by subsequent bottleneck processes.

2.4.2. Analysis of Human Resource Waste Based on LOB

The production line balance rate is only 49.65%. In industrial engineering practice, a balance rate below 70% is generally considered to indicate severe resource waste. Over half of the labor time on this line is in a non-value-added idle

state. The magnitude of this waste can be quantified by the "idle rate."

Total workstations S=18, bottleneck cycle time CT=43.089s, Within a single shift (28800s), the theoretical total invested working time capacity of the entire line is: 43.089×18=775.602s. The sum of the actual effective work times for all processes (i.e., the sum of standard times) is 385.107s. Therefore, the absolute idle time waste within a single cycle is: 775.602-385.107=390.495s.

This means that in every cycle period, 50.3% of the total line time is completely wasted. Converted to a single shift, this equates to an average of about 4 hours per workstation per day spent in a waiting state. This inefficient mode of "people waiting for machines" or "people waiting for people" directly causes labor costs to become ineffective costs.

2.4.3. Fluctuation and Flow Direction Analysis Based on SI

The smoothness index SI=23.81, This value is far higher than the ideal state (<5), revealing severe fluctuations in workload between processes. Further analyzing the direction of fluctuations reveals significant flow oscillations, specifically manifesting in the following three types of flow anomalies:

(1) Cycle Time "Cliff" Phenomenon: Between OP7 (18.92s) and OP8 (42.12s), as well as between OP17 (16.74s) and OP18 (43.09s), the time differences between consecutive processes are as high as 23.2s and 26.35s, respectively. These severe "cycle time steps" cause WIP accumulation at the downstream processes (OP8, OP18), while workers at the upstream processes (OP7, OP17) are forced to stop frequently, creating a vicious cycle of "upstream starvation, downstream congestion."

(2) Cycle Time "Valley" Phenomenon: Processes OP14 (Light Emission Test, 10.42s) and OP15 (Dot Lamp Holder, 15.84s) both belong to the very low cycle time zone, but there is no buffer station between them. Since the preceding process OP13 (Install Translucent Cover) has a high cycle time of 31.39s, OP14 and OP15 are in a prolonged "semi-starvation" state. Their equipment and personnel utilization rates are extremely low, creating static "false capacity"—meaning stations are staffed but cannot contribute effective output to the entire line.

(3) "Non-equilibrium" of Process Flow Direction: Among the 18 workstations, only five (OP8, OP11, OP13, OP16, OP18) have cycle times exceeding the overall line mean (21.4s); the remaining 13 are below the mean. This implies that the line lacks a production control point (Pacemaker); no single process can stably pull the entire flow. WIP flows quickly at low-time stations (e.g., OP1~OP7) but instantaneously accumulates at high-time stations (e.g., OP8, OP18). This increases the difficulty of on-site management and makes the entire line highly susceptible to shutdown risks due to minor production anomalies.

3. Optimization Scheme Design for the Assembly Line

Through the quantitative assessment and diagnosis of the current state of the LED assembly line in the previous sections, significant optimization potential was identified in terms of human resource utilization, workload distribution, and bottleneck constraints. In real-world industrial environments, enterprise improvement decisions are often influenced by multiple factors such as market demand fluctuations, capital budget constraints, and production cycle variations. Mere "efficiency enhancement" or "capacity expansion" often falls short of covering complex business objectives. Therefore, following the continuous improvement philosophy of Industrial Engineering (IE), this study designs two restructuring schemes with different orientations, aiming to address the production line pain points through differentiated logic. These are the efficiency-driven Scheme I and the capacity-driven Scheme II.

3.1. Process Restructuring Based on the ECRS Principle

3.1.1. Scheme I

Scheme I focuses on "stock optimization" and "cost control." Without increasing equipment investment, it deeply merges non-bottleneck processes using the ECRS principle. The goal is to compress redundant manpower and maximize the balance rate and per capita labor productivity, making it suitable for mature markets with stable demand. Specific changes include merging OP1 with OP2, OP3 with OP4, OP5 with OP6, OP9 with OP10, and OP13 with OP14 into five new workstations. Simultaneously, the original FQC inspection at OP12 is moved to after OP15 and merged with OP15. This reduces the total number of workstations from 18 to 12, netting a reduction of 6 operators. In terms of elimination and simplification, Scheme I removes unnecessary handling and waiting links between some processes and simplifies tooling and fixtures to ensure stable operational efficiency after merging. Details are shown in Table 5:

Table 5. Scheme I improvement table

Optimized Station	Included Processes	Operation Summary	Optimized Time (s)
ST1	OP1+OP2	Solder paste printing and component placement	25.826
ST2	OP3+OP4	Reflow soldering and lamp board testing	36.691
ST3	OP5+OP6	Apply thermal grease and insert board into PC tube	29.929
ST4	OP7	Thread wire through heat sink	18.921
ST5	OP8	Lamp board wire soldering	42.124
ST6	OP9+OP10	Screw board to heat sink, fix constant current board	32.622
ST7	OP11	Install lamp holder	31.647
ST8	OP13+OP14	Install translucent cover and light emission test	41.807
ST9	OP15+OP12	Dot lamp holder and FQC inspection	33.611
ST10	OP16	Visual inspection and cleaning	32.105
ST11	OP17	Functional testing	16.735
ST12	OP18	Packaging	43.089

3.1.2. Scheme II

Scheme II focuses on "incremental expansion" and "output breakthrough." Based on the Theory of Constraints (TOC), it implements process reorganization and equipment parallelization for the absolute system bottlenecks, aiming to completely break the capacity "ceiling." This is suitable for periods of surging orders or market expansion pursuing economies of scale. The specific changes involve splitting the two longest-duration processes (both exceeding 42 seconds)—the original OP8 (Lamp Board Wire Soldering) and OP18 (Packaging)—into two parallel workstations each. Simultaneously, to prevent secondary bottlenecks, the original OP11 (Install Lamp Holder), OP16 (Visual Inspection & Cleaning), and OP13 (Install Translucent Cover) are also split into parallel workstations. After significantly shortening the cycle times of these processes through parallelization, they become the new bottlenecks, while the remaining processes basically remain single workstations. These changes increase the total number of workstations from 18 to 23, adding 5 parallel stations. Details are shown in Table 6:

Table 6. Scheme II improvement table

Station	Process Name	Time (s)	Quantity
ST1	OP1 Solder Paste Printing	10.691	1
ST2	OP2 Component Placement	15.136	1
ST3	OP3 Reflow Soldering	21.05	1
ST4	OP4 Lamp Board Testing	15.641	1
ST5	OP5 Apply Thermal Grease	15.429	1
ST6	OP6 Insert Board into PC Tube	14.5	1
ST7	OP7 Thread Wire through Heat Sink	18.921	1
ST8	OP8 Lamp Board Wire Soldering	21.062	2
ST9	OP9 Screw Board to Heat Sink	16.511	1
ST10	OP10 Apply Silicone to Board	16.111	1
ST11	OP11 Install Lamp Holder	15.8235	2
ST12	OP12 FQC Inspection	17.77	1
ST13	OP13 Install Translucent Cover	15.694	2
ST14	OP14 Light Emission Test	10.419	1
ST15	OP15 Dot Lamp Holder	15.841	1
ST16	OP16 Visual Inspection & Cleaning	16.0525	2
ST17	OP17 Functional Testing	16.735	1
ST18	OP18 Packaging	21.5445	2

3.2. Theoretical Effects after Improvement

3.2.1. Calculation Process of Evaluation Indicators

(1) Theoretical Calculation for Scheme I (Efficiency-driven)

Scheme I compresses the number of workstations to 12 through process merging, reducing the total staffing to 12 people.

Bottleneck cycle time(CT_1): Determined by ST12, $CT_1 = 43.089$s.

Line of Balance (LOB_1):

$$LOB_1 = \frac{\sum T_{std}}{S \times CT_1} = \frac{385.107}{12 \times 43.089} \times 100\% \approx 74.48\%$$

Smoothness index (SI_1):

$$SI_1 = \sqrt{\frac{2244.288}{12}} = \sqrt{187.024} \approx 13.676$$

Theoretical capacity (P_1):

$$P_1 = \frac{28800}{43.089} \approx 668 \text{ units/shift}$$

(2) Theoretical Calculation for Scheme II (Capacity-expansion)

Scheme II breaks the bottleneck through parallelization, with a total staffing of 23 people. At this point, the system bottleneck is still ST18($T = 21.5445s$).

Bottleneck cycle time (CT_2): $CT_2 = 21.5445s$.

Line of Balance (LOB_2):

$$LOB_2 = \frac{385.107}{23 \times 21.5445} \times 100\% \approx 77.72\%$$

Smoothness index (SI_2):

$$SI_2 = \sqrt{\frac{633.7889}{23}} = \sqrt{27.56} \approx 5.25$$

Theoretical capacity (P_2):

$$P_2 = \frac{28800}{21.5445} \approx 1336 \text{ units/shift}$$

3.2.2. Performance Comparison Analysis Before and After Optimization

The comparison before and after optimization shows that both improvement schemes significantly alleviate the inefficiency and high waste of the original line. The original line operated with 18 workstations and a bottleneck cycle time of 43.089s, with a balance rate of only 49.65%, a smoothness index as high as 23.81, a theoretical capacity of 668 units/shift, and a per capita output of only 37.1 units, indicating severe idle manpower and cycle time fluctuations. Scheme I (efficiency-driven) compresses the workstations to 12 through process merging. Without changing the bottleneck cycle time, it increases the balance rate to 74.48%, reduces the smoothness index to about 13.68, maintains the theoretical capacity, but increases the per capita output to 55.7 units (an increase of 50%), achieving significant staff reduction and efficiency improvement. Scheme II (capacity-expansion), through parallelization of bottleneck processes, compresses the bottleneck cycle time to 21.545s, further increases the balance rate to 77.72%, brings the smoothness index close to the ideal value (about 5.25), doubles the theoretical capacity to 1336 units/shift, and increases per capita output to 58.1 units, completely breaking through the capacity limit. Overall, both schemes raise the balance rate to above 70% (a good level), effectively resolving the cycle time cliffs and flow oscillation issues. Scheme I is suitable for cost-sensitive stable markets, while Scheme II is suitable for growth-oriented expansion needs. Enterprises can flexibly choose based on their actual business strategies. Subsequently, the FlexSim simulation model will be used to dynamically verify the above theoretical calculation results.

4. FlexSim-Based Simulation Modeling and Verification

4.1. Simulation Model Construction

4.1.1. Selection of Modeling Entities and Logic

During model construction, a 1:1 restoration was performed according to the actual layout of the assembly line. The main modeling entities selected and their logical functions are defined as follows: Source: Defined as "Material Warehouse," simulating the initial input of parts, controlling the material inflow rate using Inter-Arrival Time. Processor: Simulates the 18 assembly processes. The processing time for each processor strictly maps to the standard time Tstd. determined in Chapter 2. Queue: Simulates the buffer links between processes. According to the actual on-site floor space, the maximum capacity of each Buffer is set to 10, simulating the upper limit of material accumulation before each process. See Figure 1:

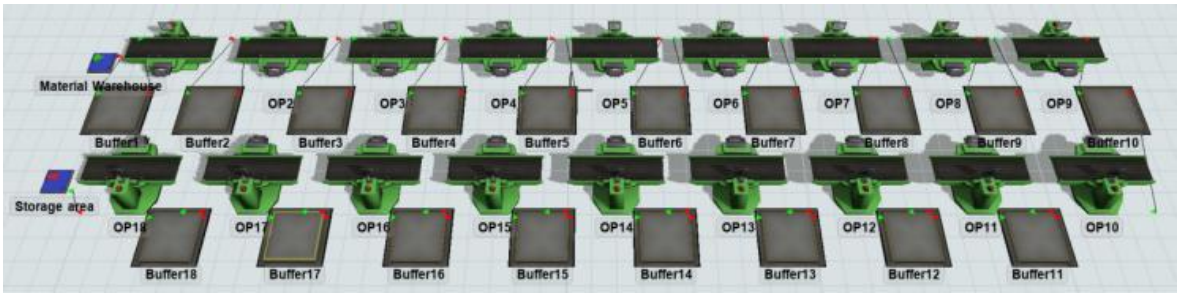

Figure 1. FlexSim 3D simulation model of the current LED lamp production line

4.1.2. Setting of Key Simulation Parameters

To ensure the statistical rigor of the simulation experiments, the operation parameters of the model were standardized as follows: The simulation running time (Run Time) is set to 28800s (i.e., an 8-hour single-shift operation duration) to observe the output under a complete shift. The Warm-up Period is set to 3600s. Since the initial state of the simulation system is empty, with high data volatility, the warm-up period removes non-steady-state data from the model's startup phase, recording statistical indicators only after the system enters a steady state. Processing distribution: To simulate random interference in real production, the processing time for each station uses not only the deterministic T_{std}, but also introduces small random fluctuations following a lognormal distribution to enhance the model's robustness. Material flow rules: Adopt the "First-In-First-Out" (FIFO) principle to ensure that product flow logic conforms to the actual process specifications of the assembly line.

4.1.3. Model Constraints and Assumptions

To focus on the core research objectives, this model sets the following assumptions: 1. Ignore instantaneous shortages in raw material supply. 2. Do not consider prolonged downtime due to extreme equipment failures (i.e., MTBF/MTTR is set to an ideal state). 3. Since a 5% fatigue allowance has already been incorporated into the standard time calculation, the simulation model does not consider efficiency fluctuations caused by fatigue curves and does not include a separate dynamic fatigue decay function.

4.2. Verification of the Current Model and Bottleneck Diagnosis

4.2.1. Model Validity Verification

Before simulating the improvement schemes, the current model must first be run and verified to ensure that the simulation environment can truly replicate actual production conditions and to deeply identify bottlenecks based on dynamic data. The simulation model was set to run for 32400s (including 3600s warm-up period). The average output data derived after 10 repeated runs are shown in Table 7:

Table 7. Model validity verification table

Evaluation Indicator	Theoretical Calculated Value	Simulation Observed Value	Error Rate
Single-shift output (P)	668	665	0.45%
Bottleneck station utilization	100%	100%	0%

As seen in the table, the error between the simulated output and the theoretical calculation results is within 0.5%, indicating that this FlexSim model has a high degree of fidelity in terms of logic modeling, parameter settings, and random fluctuation processing. It can serve as a benchmark for subsequent optimization studies.

4.2.2. Bottleneck Diagnosis Based on Simulation Data

The bar chart of current equipment utilization exported from FlexSim provides an intuitive view of the dynamic operational bottlenecks of the production system. The chart shows that the utilization rates of OP8 (Lamp Board Wire Soldering) and OP18 (Packaging) are close to 100%, operating at full capacity. This confirms that OP8 and OP18 are the "short boards" restricting the release of the line's overall capacity, and the system's overall output speed is entirely limited by the processing capability of these stations. In sharp contrast, the utilization rates of OP1, OP2, OP4, OP5, OP6, OP9, OP10, OP14, OP15, OP17, etc., are extremely low (generally below 40%). The portions representing idle and blocked time dominate their bar charts. This validates the judgment made in Chapter 2 regarding "low balance rate leading to labor redundancy," indicating that a large number of equipment and personnel are in a "waiting" state during production. The chart also shows that the utilization distribution of the production line exhibits a severe "sawtooth" pattern. This high Smoothness Index (SI) implies that in actual production, upstream stations frequently experience "blocking," while downstream stations are often in an "idle" state, resulting in extremely poor continuity of material flow. See Figure 2 for details:

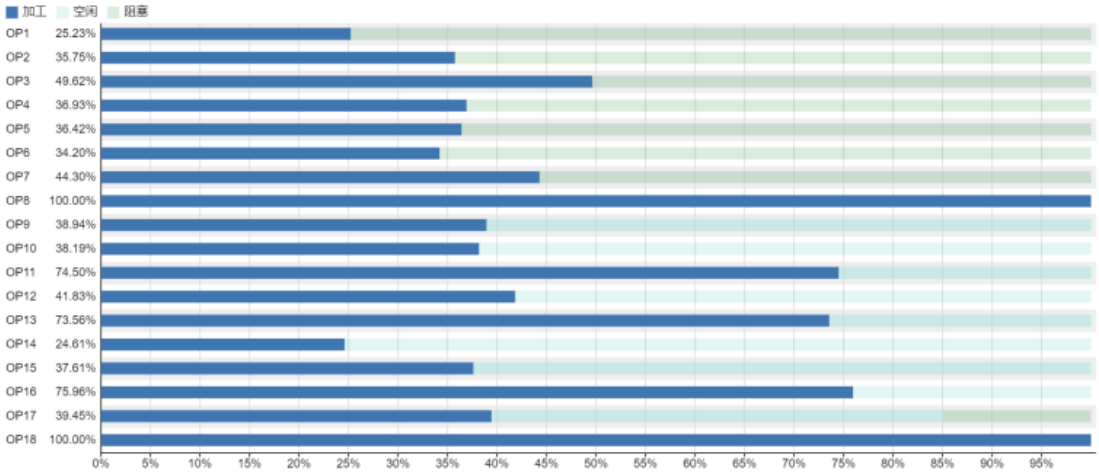

Figure 2. Statistical chart of equipment utilization for each workstation in the current state

Dark blue represents Processing, light blue represents Idle, and light green represents Blocked.

4.3. Simulation of Improvement Scheme I (Efficiency-driven)

4.3.1. Model Construction for Scheme I

Maintaining the original equipment investment unchanged, Scheme I aims to reduce labor costs and improve per capita output efficiency through merging and reorganizing non-bottleneck processes. This section verifies the dynamic performance of this "streamlined" scheme through simulation. Based on the ECRS optimization results in Section 3.1, the original 18 workstations were restructured into 12 integrated workstations (ST1-ST12) in FlexSim. These workstations merged a total of 6 processes from the original OP1, OP2, etc. The total number of Processors in the simulation model was reduced from 18 to 12. At the same time, the lognormal random fluctuation parameters and the 3600s warm-up period were kept unchanged, ensuring that the only variable in the comparative experiment was "process distribution and quantity." The specific modeling of Scheme I is shown in Figure 3:

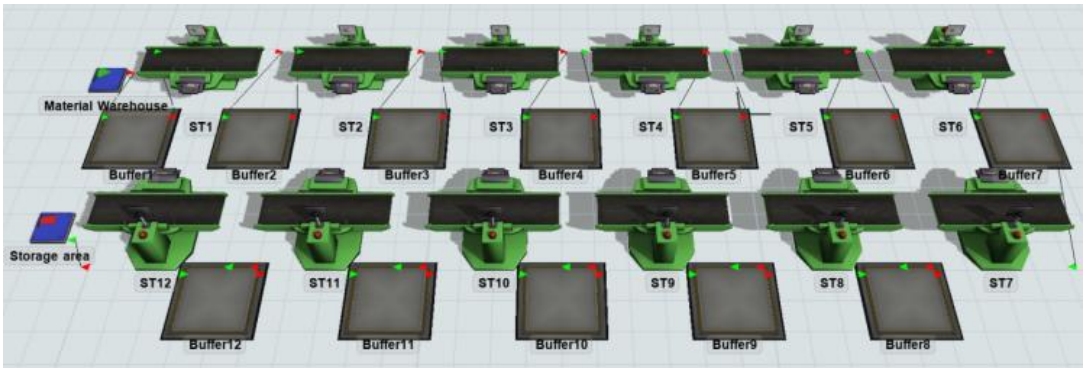

Figure 3. Simulation model layout for Scheme I (efficiency-driven) improvement

4.3.2. Utilization and System Evaluation for Scheme I

Observing the equipment utilization bar chart for Scheme I, the following conclusions can be drawn:

Load distribution becomes more reasonable: Compared to the current model, the processing proportions of non-bottleneck stations (such as ST1, ST2, ST3, ST6, ST8, ST9) have increased significantly, generally rising above 70%. This indicates that the process merging successfully eliminated the original "extreme idle" states. However, the absolute bottleneck of the system remains locked at ST12 (the original packaging station). As shown in the figure, the utilization of ST12 is still capped, which explains why Scheme I cannot fundamentally achieve a capacity leap—the system's narrowest "bottleneck neck" has not been widened.

(2) Logistics stability enhanced: Observing the blocking proportions of each station in the figure, their distribution is more uniform compared to the current model. This means that the buffers between stations are utilized more efficiently, and the smoothness of the line's cycle time has initially improved.

The specific utilization rates for each station are shown in Figure 4:

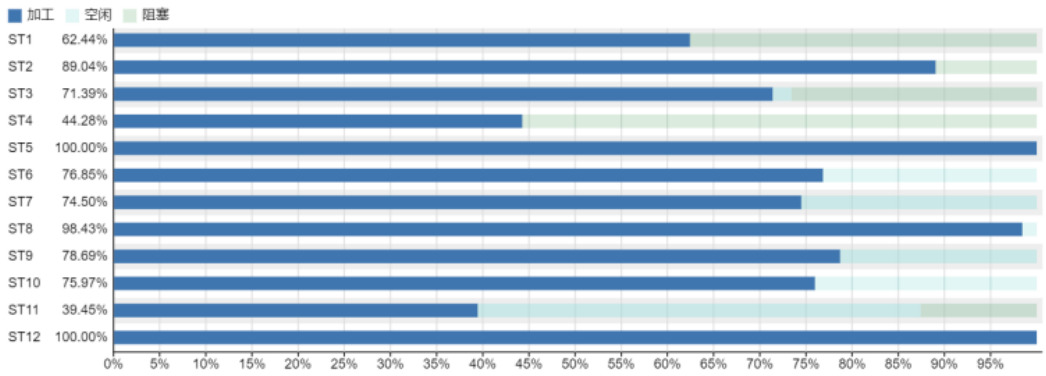

Figure 4. Statistical chart of equipment utilization for each workstation in Scheme I

4.4. Simulation of Improvement Scheme II (Capacity-expansion)

4.4.1. Model Construction for Scheme II

To ensure benchmark consistency for the comparative experiment, the Scheme II model was reconstructed using the validated current model as the base. The core improvement of Scheme II involves implementing a "space-for-time" strategy for the original bottleneck processes OP8 (Lamp Board Wire Soldering) and OP18 (Packaging). In the simulation environment, this study did not use two separate entities to represent parallelism. Instead, the maximum capacity of the built-in attributes for each parallel station was set to 2 times. This effectively reduced the equivalent cycle time of these links to roughly half of the original. The specific modeling of Scheme II is shown in Figure 5:

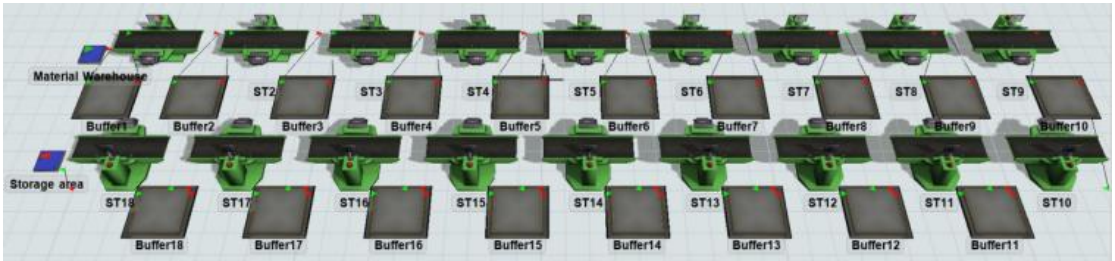

Figure 5. Simulation model layout for Scheme II (capacity-expansion) improvement

4.4.2. Utilization and System Evaluation for Scheme II

The simulation results show that Scheme II successfully broke the physical lock restricting the line's capacity by implementing parallelization transformations on the core bottleneck stations ST8 (original OP8) and ST18 (original OP18). The single-shift output achieved a leapfrog growth of approximately 100% compared to the current state. From the equipment utilization bar chart, it can be intuitively observed that the original load distribution imbalance characterized by "single-point extremely high, multiple-point extremely low" has been fundamentally reversed. Moreover, the processing proportions of the vast majority of stations across the line have significantly improved. This utilization distribution characteristic indicates that Scheme II not only successfully

unlocked production potential through the "space-for-time" strategy but also achieved an extremely high production line balance rate through process restructuring. The entire production system, while maintaining high throughput, possesses excellent logistics smoothness and operational synchronization, making it an ideal optimization scheme for handling high-intensity order demands. The specific utilization rates for each station are shown in Figure 6:

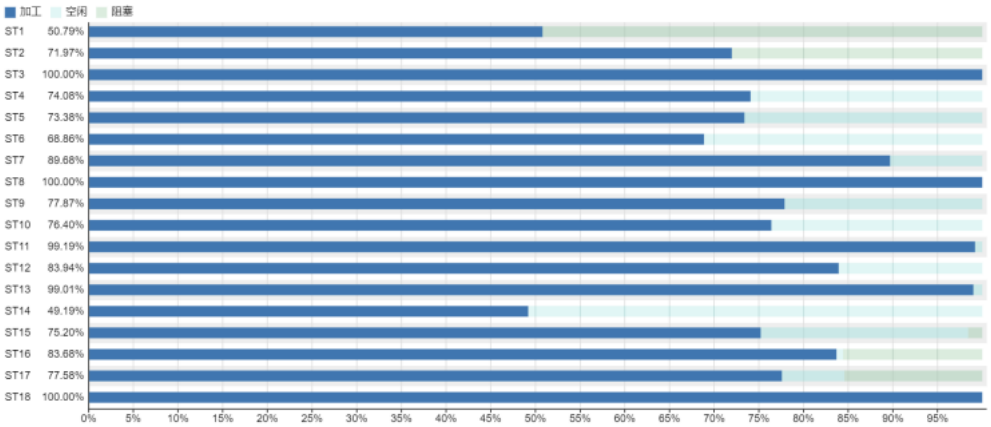

Figure 6. Statistical chart of equipment utilization for each workstation in Scheme II

5. Comparison and Evaluation of Improvement Effects

5.1. Comparison of Comprehensive Evaluation Indicators

To intuitively demonstrate the performance improvement effects of different improvement schemes on the LED lamp assembly line, this study systematically compares the current model, Scheme I (efficiency-driven), and Scheme II (capacity-expansion) from multiple dimensions, including the number of workstations, bottleneck cycle time, production line balance rate, smoothness index, theoretical capacity, per capita output, and simulated verification output. The specific indicator data are shown in Table 8:

Table 8. Comparison table of evaluation indicators

Evaluation Indicator	Current Model	Scheme I (Efficiency-driven)	Scheme II (Capacity-expansion)
Number of workstations	18	12	23
Bottleneck CT (s)	43.089	43.089	21.545
LOB (%)	49.65%	74.48%	77.72%
SI	23.81	13.68	5.25
Theoretical capacity (units/shift)	668	668	1336
Per capita output (units/person-shift)	37.1	55.7	58.1
Simulated output (units/shift)	665	664	1326

5.2. In-depth Analysis of Improvement Effects

5.2.1. Analysis of Capacity Utilization and Bottleneck Breakthrough

From the perspective of capacity utilization and bottleneck breakthrough, the bottleneck cycle time of the current line is determined by two processes—OP8 (Lamp Board Wire Soldering) and OP18 (Packaging)—forming a bimodal barrier. Its cycle time of 43.089s directly locks in the system's capacity ceiling. Simulation statistics show that the utilization rates of these two bottleneck stations are almost capped at 100%, while many upstream stations are in intermittent idle states. Although Scheme I effectively increases the work density of non-bottleneck processes through process merging, it fails to widen this physical bottleneck. Consequently, the theoretical capacity and simulated output are strictly limited to 668 units/shift, failing to achieve a magnitude leap in production capacity. In contrast, Scheme II compresses the equivalent cycle time to 21.545s by parallelizing the bottlenecks, accurately doubling the single-shift capacity to 1336 units. The simulation results (1326 units/shift) confirm this breakthrough. Scheme II completely eliminates the capacity constraint of the original line, achieving a dynamic match between resource allocation ratios and demand load.

5.2.2. Analysis of Production Balance and Process Smoothness

In terms of production line balance and process smoothness, the original line's high smoothness index of 23.81 reveals severe "sawtooth" fluctuations in workload between processes. The direct consequence is frequent blocking at upstream stations and prolonged starvation at downstream stations, resulting in extremely poor logistics continuity. Scheme I, through deep merging based on the ECRS principle, reduces the smoothness index to 13.68. Although still above the ideal value, it significantly improves the cliff-like cycle time gaps, concentrating the load across stations. Scheme II, leveraging the broad expansion brought by parallelization, further converges the smoothness index to an extremely low level of 5.25. This significantly narrows the fluctuation amplitude of loads across all stations on the line. It not only eliminates the frequent "cycle time cliff" phenomenon present in the original line but also enables the entire line to present a highly synchronized and continuously flowing "smooth cycle time" state during simulation operation, significantly reducing WIP accumulation and management difficulty.

5.2.3. Evaluation of Resource Input and Output Efficiency

From the perspective of comprehensive evaluation of resource input and output efficiency, the differentiated strategic advantages of the two schemes are particularly evident. Scheme I, without any additional fixed asset investment, reduces the number of workstations from 18 to 12 simply by optimizing work combinations. This increases per capita output from 37.1 to 55.7 units, an increase of over 50%. For cost-sensitive enterprises or those in stable market environments, this is the optimal solution for achieving "staff reduction and efficiency" and lean cost control. Scheme II, by adding 5 parallel workstations, uses a moderate increase in space and labor costs to achieve a doubled output of 1336 units/shift. Per capita output further increases to 58.1 units. Although the total staffing increases, the fixed costs allocated per unit product decrease significantly. Enterprises can

flexibly choose between these two differentiated improvement paths based on their current strategic phase of "cost priority" or "scale priority."

6. Conclusion

This study takes a certain LED lamp assembly line as its research object. Addressing the core pain points of the original line—severe idle human resources, extremely low balance rate, and limited production capacity—it systematically conducts current state diagnosis and optimization scheme design by comprehensively applying stopwatch time study, the Westinghouse Rating System, production line balancing theory, and FlexSim discrete event simulation technology. Through the current state investigation, it was found that the original line had a bottleneck cycle time as high as 43.089 seconds, a production line balance rate of only 49.65%, and a smoothness index as high as 23.81. The OP8 lamp board soldering station and the OP18 packaging station formed a bimodal bottleneck, with utilization rates close to 100%, while a large number of upstream stations had utilization rates below 40%. The line exhibited typical "cycle time cliffs" and resource redundancy. Based on this, this paper proposes two differentiated improvement strategies: The efficiency-driven scheme (Scheme I) focuses on stock optimization. It uses the ECRS principle to deeply merge and rearrange non-bottleneck processes, compressing the number of workstations from 18 to 12 without any additional equipment investment. Although it fails to change the bottleneck cycle time, it directly reduces labor costs by about 33%, increases per capita output from 37.1 to 55.7 units (an increase of over 50%), significantly raises the balance rate to 74.48%, and reduces the smoothness index to 13.68, effectively eliminating the original extreme idle and waiting waste. The capacity-expansion scheme (Scheme II), based on the Theory of Constraints, implements parallelization for the bottlenecks, successfully shortening the system cycle time to 21.545 seconds. This allows the theoretical single-shift capacity to double precisely from 668 to 1336 units, further increases the balance rate to 77.72%, brings the smoothness index close to the ideal value of 5.25, balances the utilization distribution across all stations, and increases per capita output to 58.1 units. In the simulation verification phase, the output data from FlexSim simulations strictly controlled the error with theoretical calculations to within 1%. This fully proves the scientific nature of the parameter settings and the effectiveness of the model construction, while also intuitively demonstrating the stability and robustness of the optimization schemes under dynamic logistics fluctuations. Due to research limitations, the current model makes idealized assumptions regarding complex random factors such as equipment failure rates, operator fatigue curves, and material shortages. Future research can further incorporate these dynamic variables into the model and explore the deep integration of offline simulation with workshop IoT data and Manufacturing Execution Systems (MES) to build a Digital Twin system capable of real-time warning and dynamic scheduling. Additionally, with the increasing market demand for multi-variety customization, future work can extend to research on flexible scheduling and changeover time optimization for mixed-model production, promoting the improvement of this production system from a one-time static optimization to a full-lifecycle continuous lean management approach.

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