

System-Level Energy Efficiency in High-Resolution SAR ADCs: Switching, Reference Delivery, and Digital Calibration

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Abstract: SAR ADC is suitable for sensor interfaces with strict power consumption limitations, such as biomedical, wearable devices, and the Internet of Things, due to its dynamic working mode and low power consumption. However, when the resolution of SAR ADC is increased to 14-16 bits, the power consumption and area of CDAC will sharply increase; Simultaneously reducing the size of CDAC can cause issues such as capacitor mismatch; Sampling and comparator noise both limit its energy efficiency and accuracy. This article provides an overview of key optimization techniques in high-resolution and low-power SAR ADCs. Discuss low-energy CDAC switching and charge recovery methods from two aspects: switch energy consumption and reference transient load; Analyze the collaborative design of CDAC and reference buffer, as well as the impact of reference voltage establishment error on conversion accuracy; Finally, compare the front-end and back-end calibration methods, and discuss their convergence time and trade-off with digital circuit power consumption.

Keywords: Successive-Approximation-Register ADC, Capacitive DAC, Charge Recycling, Reference Buffer, Background Calibration, Comparator Noise.

1. Introduction

In emerging application scenarios such as biomedical sensing, wearable devices, the Internet of Things, and environmental detection, the signal acquisition front-end needs to have a sufficiently high dynamic range to distinguish small signal changes, large background noise, and relatively large background signals [1, 2]. To meet the requirements, ADCs typically require a resolution of 14-16 bits [1, 2]. Among various ADC architectures, the successive approximation register analog-to-digital converter (SAR ADC) has attracted considerable attention due to its low static power consumption, relatively simple architecture, and excellent scalability of advanced CMOS technology [3, 12].

However, SAR ADC faces three main challenges.

- 1, The total capacitance of traditional binary weighted CDAC increases approximately by $2N$, thereby increasing chip area, energy consumption, and reference terminal load.
- 2, Capacitor mismatch and parasitic effects can lead to nonlinearity.
- 3, Reference voltage ripple, switch resistance, comparator noise, and kT/C noise collectively occupy a small LSB error budget [4, 6, 8]. Split, segmented, and hybrid arrays can reduce the exponential growth of capacitance, but their bridging error and inter segment error need to be controlled or calibrated [1, 2, 13].

In summary, energy efficiency should be evaluated within the complete converter boundary. Walden and Schreier quality factors can be used for performance comparison [10, 11], but if reference buffers, calibration logic, clock, or input driver power consumption are excluded, the results may be misleading. The key issue is not only which switch sequence has the lowest theoretical energy consumption, but also which CDAC switch, reference voltage supply, noise control, and calibration combination can maintain linearity with the lowest total energy consumption.

2. Switching-Energy Optimisation and Charge Reuse

2.1. Low-energy Switching Methods

CDAC switch is one of the main sources of dynamic energy consumption in SAR ADC conversion process. Compared with traditional top panel switches, monotonic switches reduce the number of capacitors that need to be charged during the conversion process and also lower the total capacitance of the capacitor array [5]. The combined capacitor switch introduces common mode voltage and adopts a stepwise switching method, further reducing the ideal conversion energy consumption [19]. In addition, reference voltage free switches and common mode switches can also reduce the voltage swing across the capacitor to lower the driving requirements for external reference sources [20]. When the unit capacitance is limited by noise and matching accuracy and cannot continue to shrink, reducing power consumption through switching methods is still an effective way to solve CDAC power consumption.

The theoretical reduction in energy consumption of a capacitor array does not necessarily mean that the power consumption of the entire SAR ADC can decrease in the same proportion. Current theoretical analysis is usually based on ideal switches and ideal reference sources, and ignores non ideal factors such as substrate parasitism [4]. In practical circuits, even if the average switching energy consumption of CDAC is already low, the capacitor array may still draw large transient currents from the reference terminal during the initial MSB judgment. The transient current will directly affect the bandwidth, driving capability, and output impedance required by the reference buffer. Therefore, when evaluating CDAC switching schemes, it is not only necessary to compare the average conversion energy consumption, but also to consider the peak current demand of the reference terminal and its impact on the power consumption of the

reference buffer [6, 16].

2.2. Charge Recycling

The charge recovery method involves reusing the stored charges in the capacitor network, rather than repeatedly releasing them to ground and re charging them from a reference source. Ginsburg and Chandrakasan reported a 37% reduction in average switch energy consumption for their analysis of a 10 bit charge recovery array [18]. Its main advantage is not only to reduce energy integration; If the charge can be redistributed between sub arrays in a controlled manner, the peak current at the reference terminal can also be reduced.

Charge reuse will also introduce new constraints. Parasitic capacitance may also cause additional charge loss, the common mode voltage during conversion may change, and the multiplexing path may require additional switching and timing phase operations. Switching resistors can also prolong the setup time. Therefore, a reliable evaluation should report the net charge extracted from each reference end, maximum current, established residuals before each comparison, and sensitivity to mismatches and parasitic effects. Overall, charge recovery can only maximize the reduction of system level power consumption by simultaneously reducing total energy consumption and the worst-case reference transient.

3. Reference-Path Co-Design

The reference voltage is usually considered an ideal voltage source, but it is also a part of the signal path in high-resolution SAR ADCs. CDAC extracts or injects a certain amount of charge from the reference network based on the digital code output by the logic circuit during each SAR bit decision process. Due to the limited output impedance and bandwidth of the actual reference network, these transient charge demands can cause a decrease in the reference voltage and a recovery process, resulting in reference voltage ripple. These errors are not equivalent to constant gain errors and may also lead to digital code loss and harmonic distortion [6]. Increasing the buffer current can improve this problem, but it will directly reduce the energy efficiency advantage of SAR architecture.

Multiple solutions have been proposed in previous research. Backend reference error calibration can estimate some establishment errors and improve the actual SNDR of high-speed SAR ADC prototypes [7]. Local energy storage capacitors or charge compensation buffers can provide short-term transient currents near CDAC; The integrated charge compensation reference buffer has been validated in sub interval SAR ADCs [21]. Another approach is to allocate more time and introduce redundancy for critical decisions, thereby relaxing the requirement for reference driving capability at a limited speed cost [16]. The calibrated 16 bit converter also utilizes energy storage capacitors and controlled reference operations to support high linearity [2].

These methods indicate that CDAC and reference buffer should be co designed based on the same transient load. The size of the buffer, energy storage, and decoupling capacitors is not designed solely based on the average current, but is designed based on the maximum charge demand and allowable establishment error under the key code pattern and decision path; Redundancy should be prioritized for decision stages with large reference switching amplitudes or slow establishment. Redundancy cannot eliminate reference noise, and energy storage capacitors also need to be charged

periodically. Therefore, the final comparison should also comprehensively consider power consumption, area, start-up time, and PVT stability.

4. Digital Calibration for High Resolution

The reduction of unit capacitance can effectively reduce the area and switching power consumption of CDAC, but it can also lead to increased capacitor mismatch and cause the actual value of capacitors in CDAC to deviate from the ideal value. Front end calibration measures the actual capacitance size during ADC startup or idle, and has been used in high-resolution SAR ADCs with split or hybrid capacitor arrays [2, 14, 17]. The disadvantage of front-end calibration is that normal conversion must be paused during calibration, so drift caused by temperature, power, or working status changes after calibration may not be corrected in a timely manner.

Digital calibration also comes with additional costs. Calibration disturbances may enter the output spectrum, coefficient convergence may be slow, and digital logic and memory may also increase power consumption and area; Moreover, algorithms can only correct errors that have been modeled and can be observed. The calibration method based on TDC can reduce the need for large auxiliary capacitor arrays, but currently the publicly available results mainly come from simulations, and its actual performance under noise and process changes still needs to be verified by chip measurements [25].

The optimal solution may not necessarily have the minimum residual error, but should achieve a more reasonable compromise between accuracy, power consumption, area, and implementation complexity.

5. Noise and Comparator Constraints

Calibration can correct deterministic errors such as weight deviation caused by capacitor mismatch, but cannot eliminate random noise. Therefore, the sampling capacitor must meet the minimum (kT/C) noise requirement, and the comparator also needs to maintain a sufficiently low false positive probability when judging small inputs close to 1 LSB [8, 15]. The comparator noise usually needs to be reduced by extending the decision time or increasing the bias current, sacrificing speed or power consumption.

In recent years, the design trend is no longer simply to increase the entire CDAC, but to redistribute capacitors and sampling functions. For example, a 13 bit SAR ADC using kT/C noise cancellation reduces the input capacitance to 240 fF and achieves 69 dB SNDR at 40 MS/s; Another 16 bit split sampling structure separates low-noise sampling from smaller and faster DACs, and achieves 93.7 dB SNDR at 5 MS/s. For SAR ADCs used in high-precision wearable scenarios, split capacitor arrays also have advantages, but require control of bridging capacitors and parasitic errors [13].

This type of technology usually adds additional working phases, gain paths, or signal processing operations, so its noise, gain errors, timing overhead, and power consumption should be included in the final evaluation criteria. For high-resolution SAR ADCs, a more meaningful metric is the total input reference noise within the target bandwidth after calibration, rather than just the nominal resolution.

6. Research Gaps and Future Directions

Although significant progress has been made in high-resolution SAR ADCs, there are still some issues that require further research. Firstly, most existing CDAC schemes focus on the average energy consumption under ideal conditions, while the design of reference buffers in practice is limited by peak current and code related transient loads. Secondly, existing calibration methods typically handle capacitor mismatch separately, but in actual circuits, reference establishment errors, comparator misalignment, and gain drift may interact with each other. Finally, the statistical range of power consumption varies among different literature, and some results do not include reference buffers and calibration logic for continuous operation, making it difficult to directly compare system level energy efficiency.

When designing CDAC, the charge variation of CDAC, reference network impedance, switch resistance, capacitor mismatch, sampling noise, and comparator noise should be analyzed uniformly. The switch scheme should not only compare the average energy consumption, but also consider the peak reference current and establishment error; The reference network should be designed based on actual transient loads and allocate more time or redundancy during important transition periods. The digital calibration criteria should mainly deal with residual errors that can be accurately observed and have a digital correction cost lower than that of analog circuits.

7. Conclusion

The design of high-resolution SAR ADC is a collaborative optimization among multiple circuit modules. Low energy switch and charge recovery technology can reduce the switching energy consumption of CDAC, but the actual effect still depends on the impact on the transient current at the reference terminal. The collaborative design of reference networks can reduce reference voltage fluctuations and establish errors, while digital calibration criteria allow for the use of smaller, lower matching accuracy analog devices, thereby further reducing area and power consumption. Sampling noise and comparator noise are random errors that cannot be completely eliminated through calibration.

Therefore, a reasonable high-resolution SAR ADC architecture should simultaneously reduce the net charge demand of CDAC and the peak current of the reference terminal, establish error tolerance through redundancy, and incorporate the power consumption of the reference buffer and calibration circuit into the overall energy consumption. The ultimate optimization goal should not be the minimum power consumption of a single module, but to achieve a system level balance between accuracy, speed, power consumption, and area.

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