

Design and Implementation of Single Phase to Three Phase AC AC Conversion System Based on AC DC AC Indirect Transformation

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Abstract: This paper designs a single-phase-input three-phase-output AC-AC conversion system adopting the indirect AC-DC-AC transformation architecture. Taking STM32G474RET6 microcontroller as the core controller, the front-stage single-phase full-bridge PWM active rectifier applies a dual-loop control combining outer-loop PI voltage regulator and inner-loop quasi-proportional-resonant (QPR) current controller to realize sinusoidal input current and high power-factor operation. The back-stage three-phase inverter adopts SVPWM modulation with feed-forward decoupling to improve DC bus voltage utilization and stabilize three-phase output voltage. Only two-line-voltage and two-phase-current signals are sampled, and the rest electrical quantities are reconstructed by calculation, which reduces hardware complexity. Functional modules including soft-start, over-voltage and over-current protection are embedded to enhance system reliability. Experimental tests show that the prototype achieves high power factor above 0.99, low total harmonic distortion of output voltage, and stable adjustable output frequency (30 Hz / 60 Hz). The proposed scheme provides a feasible technical solution for small-capacity high-performance AC-AC power conversion applications.

Keywords: AC-AC Conversion, PWM Active Rectifier, SVPWM, Dual-loop Control.

1. Introduction

Single-phase-to-three-phase power conversion is an essential technology for low-power scenarios where only single-phase AC utility is accessible, such as rural distributed power supply, mobile test platforms and small-capacity motor drives. Passive phase-conversion schemes relying on capacitors or autotransformers can hardly maintain balanced three-phase output under variable-load conditions, which restricts practical promotion. The indirect AC-DC-AC topology becomes a mainstream technical route owing to its flexible voltage-frequency adjustment capability and strong anti-disturbance performance, attracting extensive research attention in power electronics community [1-3]. Compared with single-stage matrix converters, the two-stage structure with DC-link avoids complex bidirectional-switch commutation problems and lowers hardware implementation difficulty, though it introduces extra power-conversion loss [4-5].

Numerous studies have focused on topology optimization and controller design for indirect single-phase-input three-phase-output converters. For the front-end rectifier, diode-based uncontrolled rectifier features simple hardware but suffers from serious input-current distortion and low power factor, whereas PWM active rectifier can realize sinusoidal input current and high-PF operation by adopting advanced closed-loop regulation [6-7]. For the post-stage inverter, SVPWM modulation improves DC-bus utilization compared with conventional SPWM, which is beneficial for compact prototype design under limited DC-link voltage [8-9]. Nevertheless, most existing implementations adopt full-quantity multi-sensor sampling, which increases system cost and circuit complexity; few literatures combine reduced-sensor reconstruction technology with composite

control of quasi-proportional-resonant regulator and feed-forward decoupling for small-capacity AC-AC conversion prototypes [10].

Against the above background, this paper develops a complete single-phase-to-three-phase AC-AC conversion prototype based on AC-DC-AC indirect transformation. A reduced-sampling scheme with two-line-voltage and two-phase-current measurement is adopted to reconstruct remaining electrical quantities mathematically. The front-stage applies PI-QPR dual-loop control and the back-stage uses SVPWM with feed-forward decoupling. Meanwhile, soft-start and multi-level hardware-software protection mechanisms are embedded. The main marginal contributions lie in the composite control matching the reduced-sensor sampling architecture and practical prototype verification. Experimental tests are carried out to validate power-factor performance, output-voltage quality and frequency-adjustable capacity of the constructed converter.

2. System Scheme Design and Analysis of Key Specifications

2.1. Demonstration of System Topology Scheme

Demonstration of front-end rectifier scheme: The single-phase full-bridge PWM active rectifier is selected. Although the diode rectification scheme is simple and reliable, its input current is pulsed with extremely high harmonic content, which cannot meet the requirement of $PF \geq 0.98$. The active PFC scheme adopts a PR current inner-loop to directly control the grid-side current to track the sinusoidal reference, realizing unity power-factor operation. Its Boost boost function can raise the DC-link voltage to approximately 70 V, providing sufficient voltage margin for the rear-stage

inverter. Table 1 compares various front-end rectification solutions.

Table 1. Measurement results of composite periodic-signal test

Scheme	Topology Structure	Power Factor	THD
Diode uncontrolled rectification	Single-phase diode rectifier bridge + capacitive filtering	Low	High
Single-phase full-bridge PWM active rectification	4-MOSFET full-bridge + boost inductor + DC-link capacitor	High	Low

Demonstration of Back-end Inverter Scheme: SVPWM modulation is adopted. By injecting zero-sequence components, SVPWM improves the DC-link voltage utilization ratio by about 15.5%. Under a 70 V DC-link voltage, the peak phase-voltage can reach $70/\sqrt{3} \approx 40.4\text{V}$, satisfying the output requirement of 32 V line-to-line voltage (peak phase-voltage approx. 26.1 V), with a modulation ratio of about 0.65 and sufficient margin. In practical code

implementation, the maximum and minimum values of three-phase modulation waves are calculated, and the average value is inverted and superimposed as the zero-sequence component for injection. Compared with conventional SVPWM that requires sector judgment and vector-time calculation, this algorithm only needs three comparisons and one averaging operation. It features low complexity and is suitable for 20 kHz real-time computation on the STM32G474 platform. Table 2 is the Comparison of backend inverter solutions. Figure 1 shows the block diagram of an AC-DC-AC system.

Table 2. Comparison of back-end inverter schemes

Scheme	Topology	DC-link voltage utilization ratio (phase-voltage peak value/ V_{dc})
Three-phase SPWM inverter	Three-phase six-switch bridge + LC filter	0.5
Three-phase SVPWM inverter	Three-phase six-switch bridge + LC filter	0.577

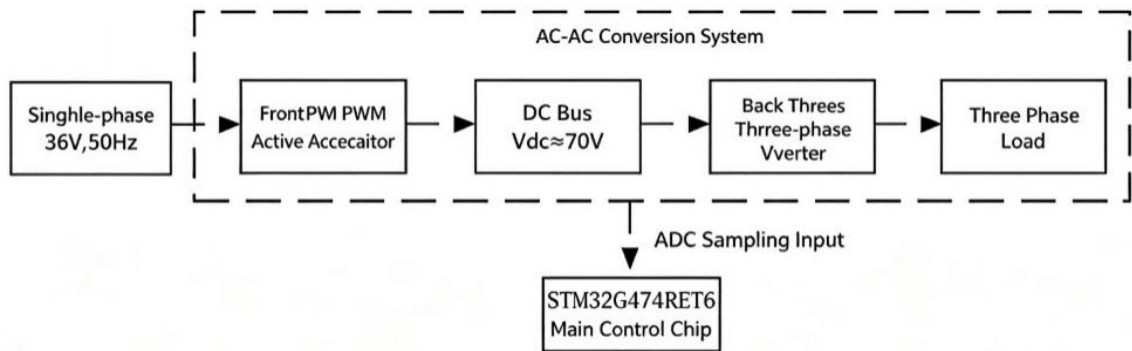


Figure 1. AC-DC-AC system block diagram

Demonstration of Sampling Scheme: The scheme of two line-to-line voltages plus two phase-currents is adopted. In a three-phase three-wire system, the sum of three-phase currents is zero and the sum of three-phase line-to-line voltages is zero. Therefore, only two line-to-line voltages (U_{ab} , U_{bc}) and two phase-currents (I_a , I_c) need to be measured, and the third quantity can be reconstructed via calculation. This scheme retains complete information required for control while reducing two sensor channels, lowering hardware cost and sampling-circuit complexity. Table 3 compares the sampling schemes. Figure 2 shows the main circuit topology.

Table 3. Comparison of sampling schemes

Scheme	Number of Sensors	Advantages and Disadvantages
Three-phase phase-voltage + three-phase phase-current	6	Complete information yet high cost
Two line-to-line voltages + two phase-currents	4	Reconstruct the third phase based on $i_a+i_b+i_c=0$ in three-wire system

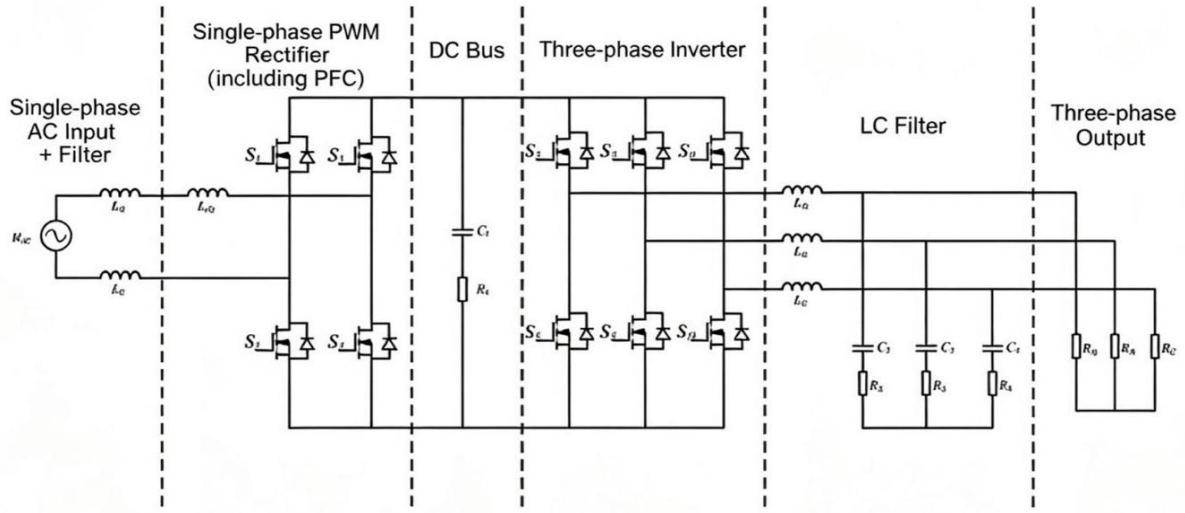


Figure 2. Main circuit topology

2.2. Demonstration of Control Strategy Scheme

Front-end PFC control scheme: The rectifier adopts a double-loop cascade control architecture. The outer voltage loop uses a PI controller to stabilize the DC-link voltage at 70 V. It increases power absorption when the DC-link voltage is low and reduces power absorption when the voltage is high. An anti-saturation mechanism is equipped to prevent integral overshoot.

The current reference output from the outer loop is sent to the current inner-loop after synchronous transformation. A quasi-proportional-resonant (QPR) controller is selected to make the inductor current accurately track the sinusoidal reference. The QPR controller achieves high gain near the resonant frequency to precisely lock the 50 Hz power frequency, while maintaining a certain bandwidth to

accommodate grid-frequency fluctuations. Parameter settings: $K_p = 6.0$, which determines system bandwidth and dynamic response speed; $K_r = 40.0$, which determines gain at 50 Hz. Larger K_r yields smaller steady-state error, yet excessive value may cause oscillation; $BW = 1, \text{Hz}$, balancing frequency adaptability and selectivity. The 1 Hz bandwidth covers ± 1 Hz grid-frequency deviation.

Finally, grid voltage feed-forward is directly superimposed onto the bridge-arm voltage reference, so that the inner loop only needs to output small correction quantities, greatly reducing control burden. DC-link decoupling eliminates the influence of DC-link voltage fluctuation on modulation gain via normalization processing, ensuring consistent control-system performance across the full voltage range. Figure 3 shows the front-end rectifier control scheme.

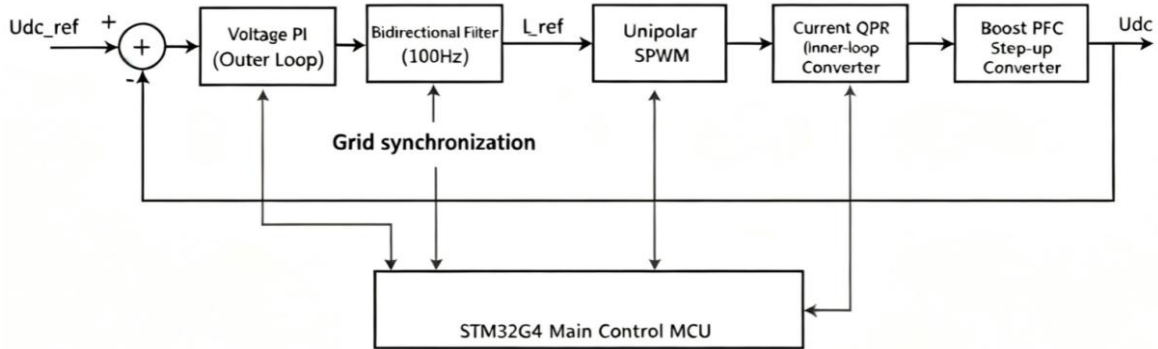


Figure 3. Front-end rectifier control scheme

Back-end three-phase inverter control scheme: The control objectives of the rear-stage three-phase inverter are: stabilize output line-to-line voltage amplitude at 32 V; support on-line switching of output frequency between 60 Hz and 30 Hz; keep output waveform $\text{THD} \leq 2\%$; resist load and input-voltage disturbances. A control structure combining single-loop PI for line-to-line voltage RMS and SVPWM feed-forward decoupling is adopted.

A single-loop PI voltage controller takes the RMS value of output line-to-line voltage as feedback and outputs the peak reference of three-phase phase-voltages M . After SVPWM modulation with $1/\sqrt{V_{dc}}$ feed-forward decoupling, the three-phase inverter bridge is driven. Compared with the PR

double-loop scheme which requires extra three-phase current sampling and double-loop parameter tuning, the PI single-loop scheme only needs to detect one line-to-line voltage and DC-link voltage, reducing sensor count to two with simple parameter tuning. Under resistive loads, the PI integral action can effectively eliminate steady-state voltage error. Combined with SVPWM feed-forward decoupling (duty-cycle normalization divided by DC-link voltage), stable output voltage is maintained under input-voltage fluctuation from 31 V to 41 V, satisfying voltage-regulation requirements. A soft-start function (0.5 s linear ramp-up) is implemented to avoid startup inrush current. Figure 4 shows the backend inverter control scheme.

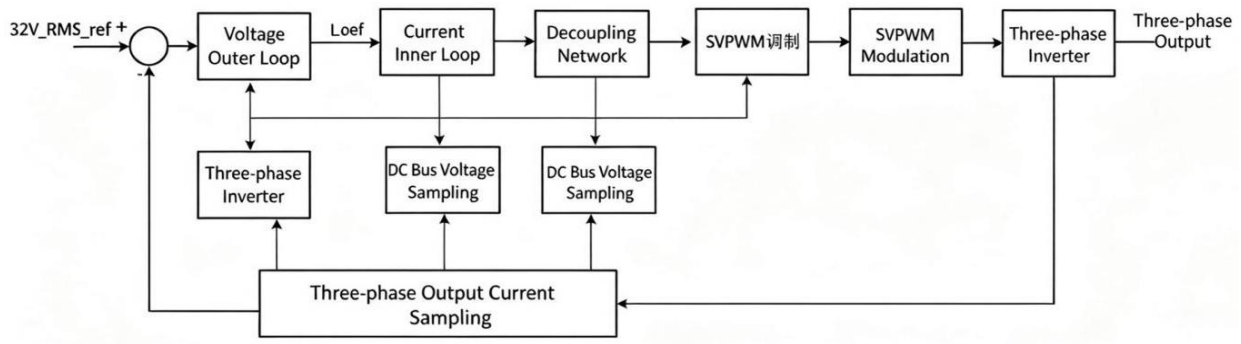


Figure 4. Back-end inverter control scheme

2.3. Design of Output LC Filter

The rear-stage requires an output line-to-line voltage of 32 V (RMS). The peak phase-voltage is $U_{phk} = (32/\sqrt{3}) \times \sqrt{2} \approx 26.13, V$. The maximum peak phase-voltage in the linear modulation region of SVPWM is $V_{dc}/\sqrt{3}$, so $V_{dc} = 26.13 \times \sqrt{3} \approx 45.26, V$. Considering switch voltage drop, dead-time loss and modulation margin, 70 V is selected. At this point, the modulation ratio $m = 45.26/70 \approx 0.65$, falling within the linear region.

An LC low-pass filter is adopted at the inverter output to filter high-frequency switching harmonics generated by SVPWM. Given a switching frequency of 10 kHz and

fundamental output frequency of 60 Hz, the filter cutoff frequency is set to 1.3 kHz. Calculated from the cutoff-frequency formula, each-phase filter inductor $L_f = 0.5, mH$ and filter capacitor $C_f \approx 30, \mu F$. Delta-connected capacitors are used, with $10, \mu F$ per phase, equivalent to $30, \mu F$ in Y-connection, consistent with theoretical calculation. To suppress LC resonance, an RC damping network is connected in parallel with filter capacitors, consisting of a $10, k\Omega$ resistor and $100, nF$ capacitor forming a symmetrical damping branch. This improves system stability and reduces output-voltage THD. Figure 5 shows a schematic diagram of the power stage and the output LC filter. Table 4: Power Device Selection

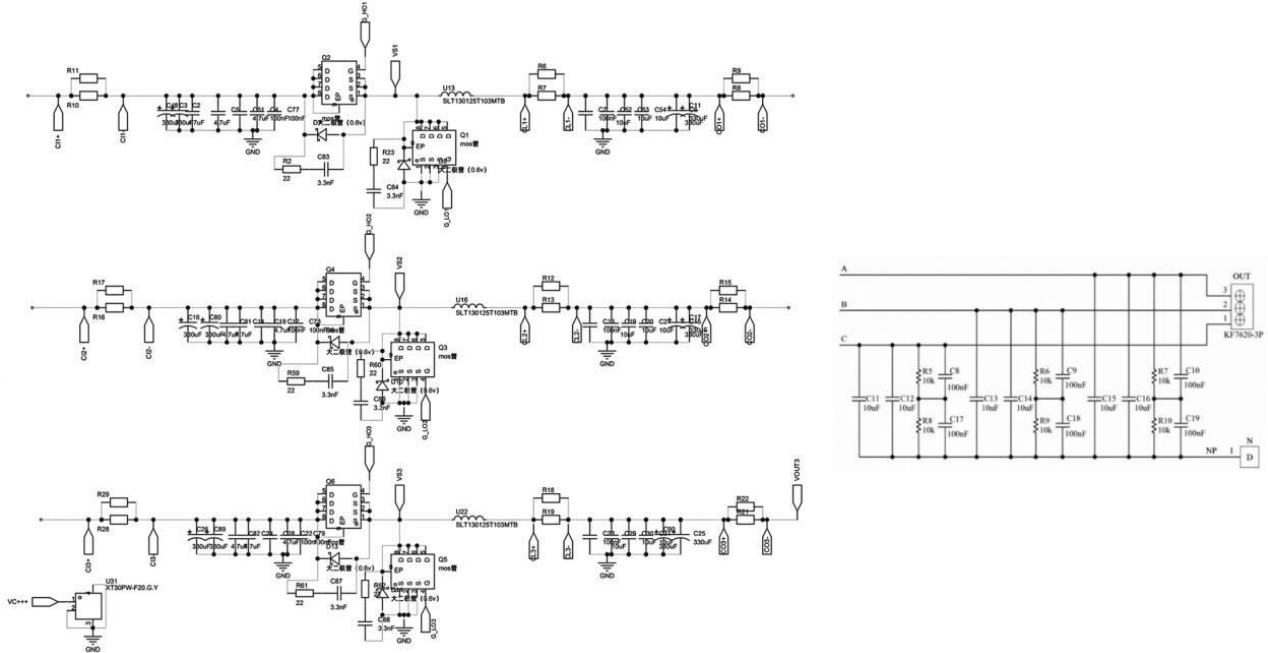


Figure 5. Schematic diagram of power stage and output LC filter

Table 4. Comparison of sampling schemes

Component	Parameter Requirements	Selected Model
Front-end MOSFET	$V_{DS}=80, V, I_D=318, A, R_{DS(on)}=7, m\Omega$	BSC0805LS
Back-end MOSFET	Same as above	Same as above
Front-end PFC inductor	300, μH	Fe-Si-Al magnetic ring
DC-link capacitor	990, μF	Multiple electrolytic capacitors in parallel
Output filter inductor	1, mH, $DCR \leq 0.1, \Omega$	SLT130125T103MTB toroidal-winding power inductor
Output filter capacitor	$3 \times 470, \mu F/16, V$ electrolytic capacitors in parallel with $10, \mu F + 0.1, \mu F$ ceramic capacitors	HGC1206R5106K500NSPJ, 100YXJ330M1

3. Software Design and System Testing

STM32G474RET6 is chosen as the main-control chip. It features a main frequency up to 170 MHz, integrated FPU, DSP instruction set, as well as CORDIC and FMAC math accelerators, which can efficiently execute real-time control and complex algorithm computation. It integrates high-resolution timers for precise PWM output regulation. On-chip resources include 5 groups of 12-bit ADC supporting differential sampling, 4 groups of 12-bit DAC, 6 operational amplifiers and 7 comparators. Abundant analog resources greatly simplify external conditioning circuits.

3.1. Front-End Single-Phase Rectifier

The software for front-end PWM rectifier is developed on the STM32 platform with C language. HRTIM high-resolution timer triggers ADC synchronous sampling to realize 20 kHz digital control. The software consists of initialization configuration layer, real-time control interrupt layer and background task layer. Within a 50 μ s control period, the system completes sampling, protection judgment, state-machine control, DC-link voltage filtering, PI outer-voltage loop and QPR inner-current-loop control, voltage feed-forward decoupling and SPWM update. Background tasks handle waveform display, status monitoring and key-button processing.

A zero-crossing startup strategy is adopted: PWM is turned off at grid-voltage zero-crossing points to realize zero-current soft-start. Protection measures including over-current, over-voltage, modulation limitation, duty-cycle boundary and zero-crossing protection are implemented to enhance system reliability. Protection actions are completed within one control cycle and immediately shut down PWM output.

3.2. Back-end Three-Phase Inverter

The back-end three-phase inverter software includes initialization configuration layer, real-time control interrupt layer and background management layer. During initialization, peripheral configuration, RMS calculation and PI-parameter setup are finished. In the real-time control layer,

within a 50 μ s cycle, voltage sampling, protection judgment, RMS calculation, PI voltage-loop regulation, three-phase sinusoidal reference generation, SVPWM modulation and duty-cycle update are performed. The background management layer is responsible for start-stop control, output-parameter adjustment and fault handling.

The system is equipped with DC-link over-voltage, under-voltage, ADC-abnormality and over-modulation protection. Protection status is monitored in real time and PWM output is shut down. A 0.5 s linear soft-start strategy limits output-voltage amplitude variation to avoid startup shock and improve system stability.

3.3. System Testing

Under input voltage $U_i = 36$, V, 50, Hz and load current $I_o = 2$, A, tests are carried out on output voltage, frequency, current, input power factor, efficiency and output-voltage THD. The output frequency is further switched to 30 Hz. Voltage regulation rate and load regulation rate are measured and recorded to evaluate dynamic regulation performance of the system. Table 5 is a test data recording form. Figure 6 shows a photograph of the experimental system.

Table 5. Test data record table

Test Item	Requirement	Measured Value
Output line-to-line voltage U_o (60 Hz)	32, V $\pm$ 0.1, V	32.06 V
Output frequency f_o (60 Hz)	60 $\pm$ 0.2, Hz	60.0 Hz
Load current I_o	2.0 A	2.001 A
Input power factor PF	$\geq$ 0.98	0.998
Efficiency η	$\geq$ 95	85%
THD	$\leq$ 2	0.4%
U_o (30 Hz)	32, V $\pm$ 0.1, V	32.05 V
f_o (30 Hz)	30 $\pm$ 0.2, Hz	30.0 Hz
Load regulation rate SI	$\leq$ 0.3	0.097%
Voltage regulation rate SU	$\leq$ 0.3	0.22%

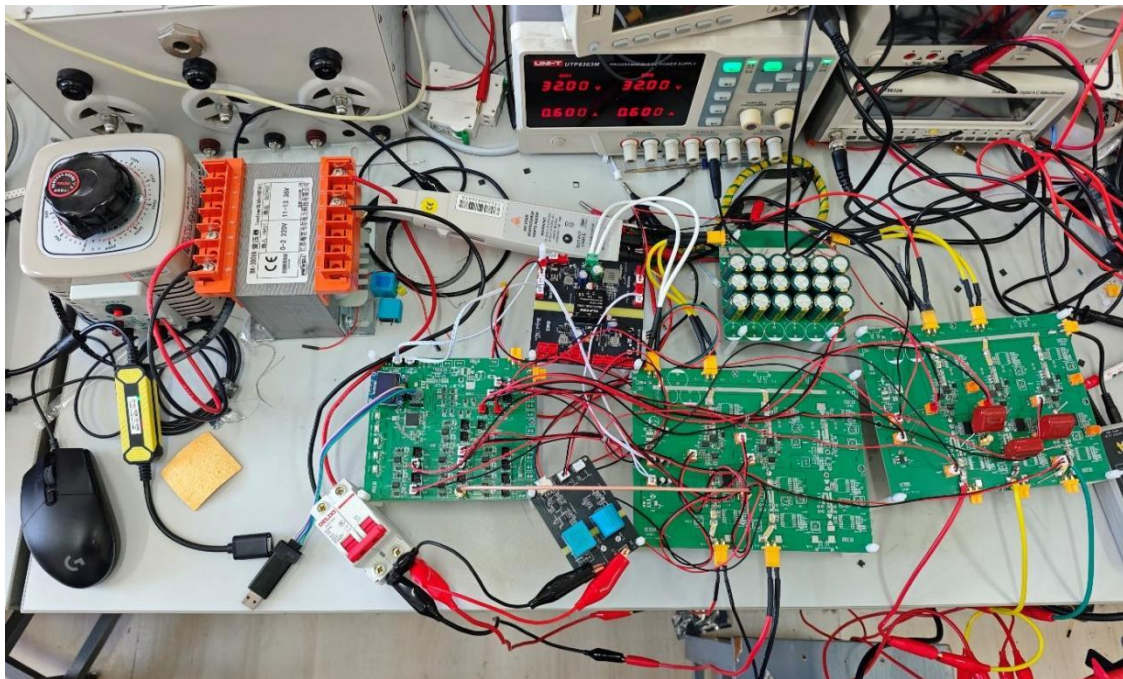


Figure 6. Experimental system diagram

4. Conclusions

This paper designs and implements a single-phase to three-phase AC-DC-AC indirect conversion system with optimized topology, control strategy and hardware parameters. By adopting a front-end PWM active rectifier with PI-QPR dual-loop control and a back-end SVPWM inverter with feedforward decoupling, the system realizes high power factor operation, low harmonic output and adjustable dual-frequency output. The optimized reduced-sensor sampling scheme effectively reduces hardware cost and circuit complexity, while the embedded soft-start and multi-level protection mechanisms significantly improve the operational stability and safety of the converter. Experimental results verify that the developed prototype achieves excellent static and dynamic performance, including a power factor higher than 0.99, extremely low output voltage THD, and superior voltage and load regulation accuracy. With compact structure, reliable operation and flexible frequency regulation capability, the proposed AC-AC conversion scheme possesses strong practical feasibility and application value, which can be widely applied in small-capacity power conversion scenarios such as rural single-phase power supply conversion, mobile experimental power platforms and low-power three-phase motor drive systems.

Despite the promising steady-state performance of the developed AC-DC-AC conversion prototype, this study still has several deficiencies. The system validation is limited to conventional working conditions, lacking verification of extreme condition adaptability and long-term operational stability, and the overall hardware efficiency can be further optimized. Future research will focus on comprehensive performance improvement and engineering promotion. Advanced adaptive control algorithms will be introduced to strengthen the system's anti-interference capability against complex grid fluctuations and sudden load changes. Extended experiments including long-term continuous operation and extreme working condition tests will be implemented to further validate and enhance the system reliability. In addition, modular structural optimization and universal parameter tuning strategies will be explored to improve the versatility and practicability of the converter, so as to provide reliable

technical support for the large-scale engineering application and popularization of single-phase to three-phase power conversion equipment in distributed power supply, mobile test platforms and motor drive fields.

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